This listing of claims replaces all prior listings of the claims in the application.

In the Claims

1. (withdrawn) A method of forming bitlines for a memory cell array of an integrated circuit and conductive lines interconnecting transistors of an external region outside of said memory cell array, comprising:

patterning troughs in a dielectric region covering said memory cell array according to a first critical dimension mask only;

forming bitline contacts to a substrate and bitlines in said troughs; and

forming conductive lines consisting essentially of at least one material selected from the group consisting of metals and conductive compounds of metals in horizontally oriented patterns patterned by a second critical dimension mask, said conductive lines interconnecting said bitlines to transistors of external circuitry outside of said memory cell array, said conductive lines being interconnected to said bitlines only at peripheral edges of said memory cell array.

2. (withdrawn) The method of claim 1 wherein said bitline contacts are formed borderlessly to wordlines coupled to said memory cell array, said wordlines being encapsulated by insulative material.

3. (withdrawn) The method of claim 1, wherein said bitline contacts include a first layer consisting essentially of polysilicon and said bitlines include a second layer

consisting essentially of at least one material selected from the group consisting of metals and conductive compounds of metals.

4. (withdrawn) The method of claim 3 wherein said second layer is formed by etching back said first layer in said troughs and then simultaneously depositing said at least one material selected from the group consisting of metals and conductive compounds of metals while depositing said at least one material in said horizontally oriented patterns to form said conductive lines.

5. (withdrawn) The method of claim 2 wherein said bitlines and said bitline contacts consist essentially of at least one material selected from the group consisting of metals and conductive compounds of metals.

6. (withdrawn) The method of claim 5 wherein said first critical dimension mask includes elongated line-space patterns such that said troughs extend linearly across a multiplicity of said encapsulated wordlines.

7. (withdrawn) The method of claim 6 wherein said conductive lines are broader than said bitlines where said conductive lines interconnect to said bitlines.

8. (withdrawn) The method of claim 7 wherein said conductive lines interconnect pairs of said bitlines to sense amplifiers located in said external regions beyond opposite edges of said memory cell array, wherein successive pairs of said

bitlines are coupled to sense amplifiers located in alternating ones of said external regions.

9. (withdrawn) The method of claim 8 wherein said interconnections between said conductive lines and said bitlines are formed over isolation structures substantially unaffected by patterning of said troughs and said horizontally extending patterns.

10. (withdrawn) The method of claim 1 further comprising forming vertically extending patterns in said external region prior to forming said horizontally extending patterns, at least some of said vertically extending patterns contacting said substrate, and simultaneously filling said troughs, said vertically extending patterns and said horizontally extending patterns to form conductive contacts and said conductive lines.

11. (withdrawn) A method of forming contacts to a substrate of an integrated circuit (IC) for an array of memory cells and for external circuitry outside of said array, comprising:

forming an array of memory cells in an array portion of a substrate, each cell including a storage capacitor and an array transistor;

forming encapsulated wordlines for operating said memory cells;

forming external transistors in an external portion of said substrate outside of said array portion;

forming a dielectric layer covering said array of memory cells and said external transistors;

forming troughs in said dielectric layer in said array portion; said troughs running in a direction transverse to said wordlines;

forming array contacts in said troughs, said array contacts extending to said substrate;

forming bitlines in said troughs above said array contacts, said bitlines including at least one material selected from the group consisting of metals and conductive compounds of metals;

forming external contacts to said substrate in said external portion of said substrate; and

simultaneously forming conductive interconnects between ones of said external transistors and between said bitlines and said external transistors.

forming a conductor layer in said troughs including a material selected from the group consisting of metals and conductive compounds of metals;

forming external contacts to said single-crystal semiconductor in said external region; and

simultaneously forming conductive interconnects between ones of said external transistors and between said conductor layer and said external transistors.

12. (currently amended) An integrated circuit ~~including a memory cell array and an external region outside of said memory cell array,~~ comprising:

a substrate having a single-crystal semiconductor region defining a major surface of said substrate;

a plurality of first transistors having conduction channels disposed in a memory cell array region of said semiconductor region;

a plurality of second transistors having conduction channels disposed in an external region of said semiconductor region outside of said memory cell array region;

a dielectric region covering said first transistors and said second transistors, said dielectric region having a plurality of troughs, each said trough having a pair of vertical sidewalls, each said sidewall extending substantially in a single plane to said substrate;

a plurality of bitline contacts disposed in said troughs, said bitline contacts including a plurality of conductive vias extending in a vertical direction normal to said major surface to contact said first transistors;

~~to a substrate and~~ a plurality of horizontally extending bitlines disposed in said troughs and conductively connected to said conductive vias, said bitlines extending over said memory cell array region in a horizontal direction substantially parallel to said major surface~~disposed in said memory cell array~~; and

metallic conductive lines interconnecting said bitlines to said second transistors, said conductive lines differing from said bitlines in a patterned characteristic including at least one of horizontal width, vertical thickness, and placement relative to said bitlines~~being patterned separately from said bitlines~~.

13. (canceled)

14. (currently amended) The integrated circuit of claim ~~13~~12 ~~further comprising conductive interconnections interconnecting~~ wherein said bitlines are interconnected to said conductive lines by a plurality of horizontally disposed conductive interconnections, said conductive interconnections differing from said bitlines in a pattern characteristic including at least one of horizontal width, vertical thickness, and placement relative to said bitlines~~to said external transistors, said conductive interconnections being patterned simultaneously with said conductive lines~~.

15. (currently amended) The integrated circuit of claim 14 further comprising wordlines encapsulated by insulative material, wherein said conductive vias of said bitline contacts include borderless contacts disposed between said encapsulated wordlines.

16. (currently amended) The integrated circuit of claim 15 wherein said conductive vias of said bitline contacts include at least a first layer consisting essentially of polysilicon and said bitlines include at least a second layer consisting essentially of at least one material selected from the group consisting of metals and conductive compounds of metals.

17. (currently amended) The integrated circuit of claim 15 wherein said bitlines and said conductive vias of said bitline contacts consist essentially of at least one material selected from the group consisting of metals and conductive compounds of metals.

18. (original) The integrated circuit of claim 17 wherein said conductive lines are broader than said bitlines where said conductive lines interconnect to said bitlines.

19. (currently amended) The integrated circuit of claim 18 wherein said conductive lines interconnect pairs of said bitlines to sense amplifiers located in a plurality of said external regions disposed beyond opposite edges of said memory cell array, wherein successive pairs of said bitlines are coupled to sense amplifiers located in alternating ones of said external regions.

20. (currently amended) The integrated circuit of claim 19 wherein said conductive interconnections ~~between said conductive lines and said bitlines~~ are disposed over isolation structures, said isolation structures isolating said memory cell array region from said external regions~~substrate from said bitlines and said conductive lines~~.